Avid Systems, Inc
Wireless E1 Monitoring System
Users Manual

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1.0 Introduction

The Wireless E1 Monitoring System consists of the AVS-1025 E1 transmitter and the AVS-1026 E1 receiver. This system is capable of transmitting and receiving two full rate E1 links for monitoring purposes.

The Wireless E1 Monitoring System transmits two E1 links over a selectable 4.72 Msps QPSK channel or a 47.2 Mcps Direct Sequence Spread Spectrum channel. The mode in which the system operates is set in both the transmitter and receiver equipment. The transmitter is configured using a web based interface that is served from the transmitter using a crossover cable to a laptop computer.

The receiver is configured using a JAVA based GUI that can run either locally on the AVS-1026 chassis or remotely. The receiver down converts, demodulates and decodes the Wireless E1 signal and outputs the E1 data links on an Ethernet connection via UDP.

2.0 AVS-1025 E1 Transmitter

The AVS-1025 E1 Transmitter is housed in a portable aluminum chassis. The transmitter is able to simultaneously monitor two E1 channels and use either QPSK or CDMA modulation schemes to transmit the E1 links to the AVS-1026 receiver. The transmitter can also be configured over a web control interface. Figure #1 depicts the AVS-1025 transmitter.

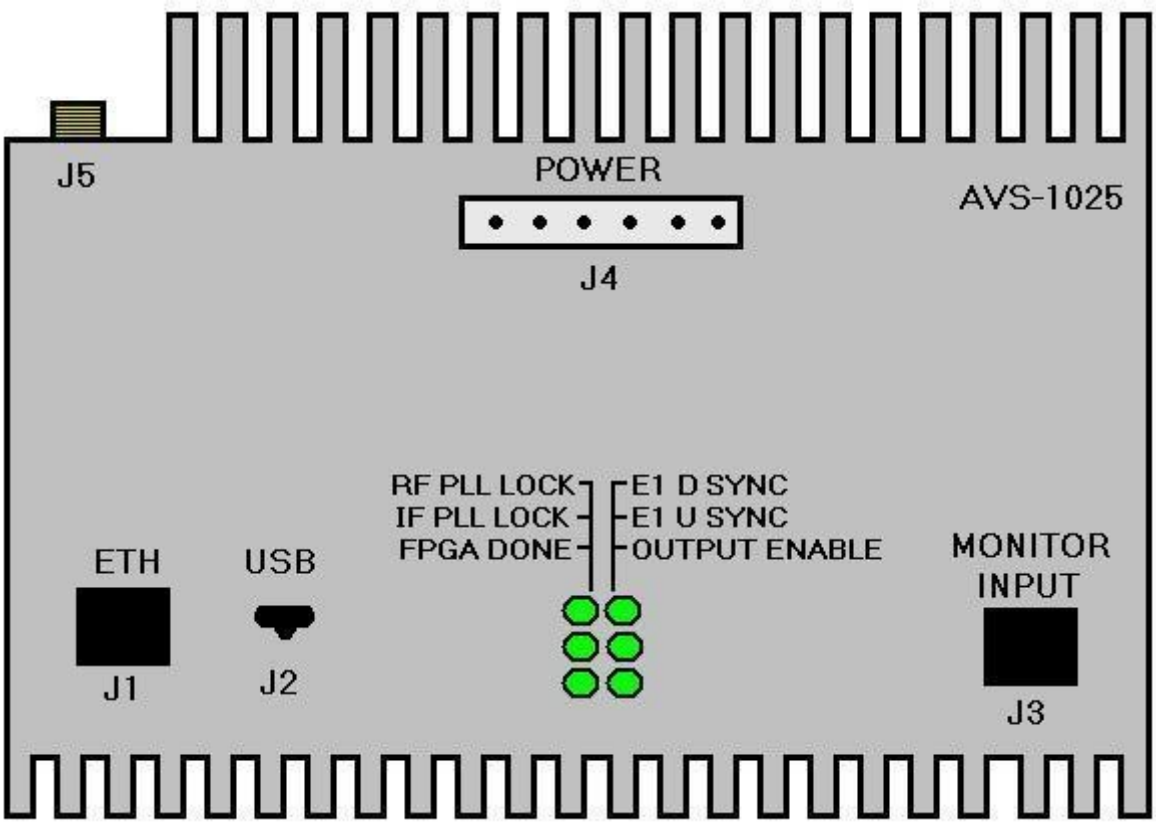


Figure #1 – AVS-1025 Transmitter

2.1 AVS-1025 Monitor Input Connector Pin Definitions

The two E1 data links are input on J3 of the AVS-1025 through the RJ-45 connector labeled MONITOR INPUT. The pin definitions of the J3 connector are shown in Table #1

Pin	Tip/Ring	Port
1	Ring 1	Port 0 – E1 U Sync
2	Tip 1	Port 0 – E1 U Sync
3	Ring 2	Port 1 – E1 D Sync
6	Tip 2	Port 1 – E1 D Sync

Table #1 – J3 Monitor Input Pin Definitions

For the remainder of this document, Port 0 is synonymous with the E1 up-link and Port 1 the E1 down-link.

2.2 AVS-1025 Power Connector

The AVS-1025 requires 12V and 5V DC power and typically draws 0.9 and 2.3 amps respectively. Table #2 describes the power connector, J4, for the AVS-1025 transmitter.

Pin	Voltage	Current
1	+5 V DC	1.15 amps
2	+ 5 V DC	1.15 amps
3	GND	
4	GND	
5	+12 V DC	.45 amps
6	+12 V DC	.45 amps
Total Power		**22.3 Watts**

Table #2 – J4 AVS-1025 Power Connector

The AVS-1025 can be controlled and configured through it's embedded web interface and will power up in the same configuration it was last powered down in. The web server is accessed through the J1 Ethernet port at the IP address defined in the delivery documentation. When connecting to the AVS-1025 directly from a PC (not through a network switch) a crossover cable must be used.

Connecting to the AVS-1025 web server will display the top level page shown below.

2.3 AVS-1025 Web Control Interface

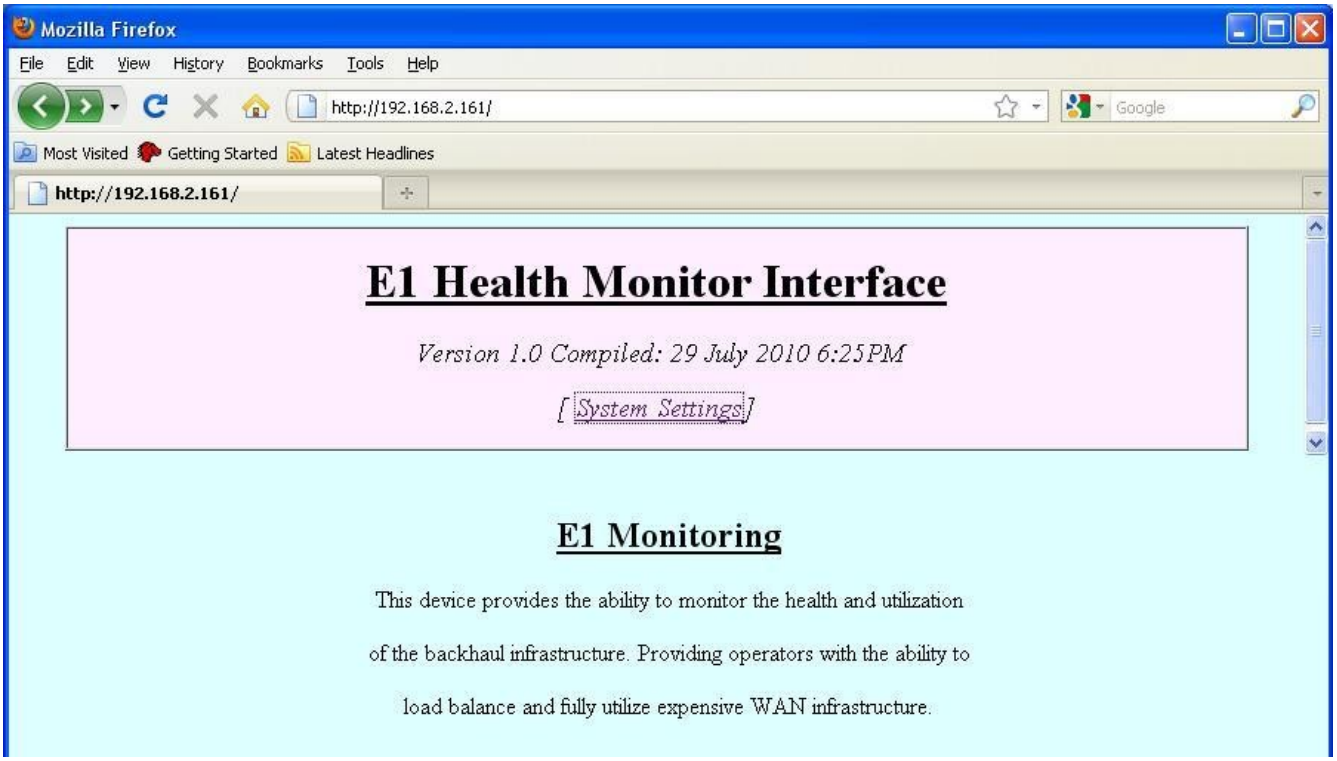


Figure #2 – AVS-1025 Web Control Interface

The "System Settings" link will take the user to the configuration page as follows below.

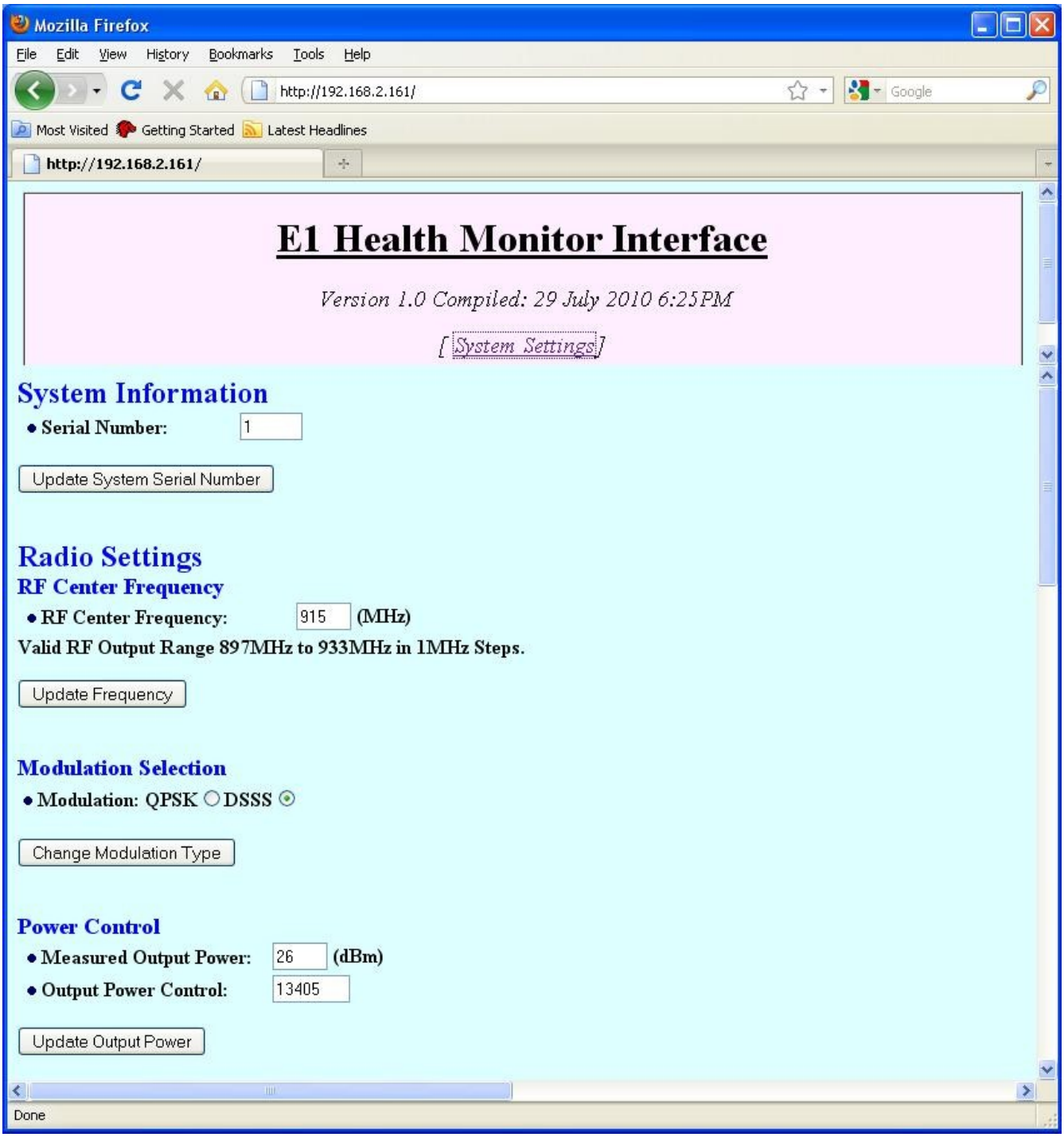

Mozilla Firefox
File Edit View History Bookmarks Tools Help
http://192.168.2.161/
Google
Most Visited Getting Started Latest Headlines
http://192.168.2.161/
E1 Health Monitor Interface
Version 1.0 Compiled: 29 July 2010 6:25PM
[System Settings]
System Information
• Serial Number: 1
Update System Serial Number
Radio Settings
RF Center Frequency
• RF Center Frequency: 915 (MHz)
Valid RF Output Range 897MHz to 933MHz in 1MHz Steps.
Update Frequency
Modulation Selection
• Modulation: QPSK DSSS
Change Modulation Type
Power Control
• Measured Output Power: 26 (dBm)
• Output Power Control: 13405
Update Output Power
Done

Figure #3 – AVS-1025 System Information and Radio Settings

The web page served from the AVS-1025 updates all fields when the system settings field is clicked on. The user will update or change the settings in the AVS-1025 whenever one of the buttons such as Update System Serial Number is depressed. The user should use care before depressing any of these buttons shown in the figure above.

System Serial Number – This field displays the serial number of the AVS-1025. The Update System Serial Number button is used to set the serial number of the unit and should not be changed after delivery.

RF Center Frequency – When the system settings field is clicked this field is updated with the current center frequency. The center frequency can be changed from 897 to 933 MHz in one MHz steps. The center frequency should be set to 915 MHz.

Modulation Selection – This field selects either QPSK or Direct Sequence Spread Spectrum as the modulation scheme of the transmitted signal. The user sets the modulation type by selecting either QPSK or DSSS then clicking on the change modulation type button.

Power Control – The current transmit power is displayed when the system settings field is clicked. The output power control field contains value that adjusts the bias voltage to the power amplifier. This value should not be changed.

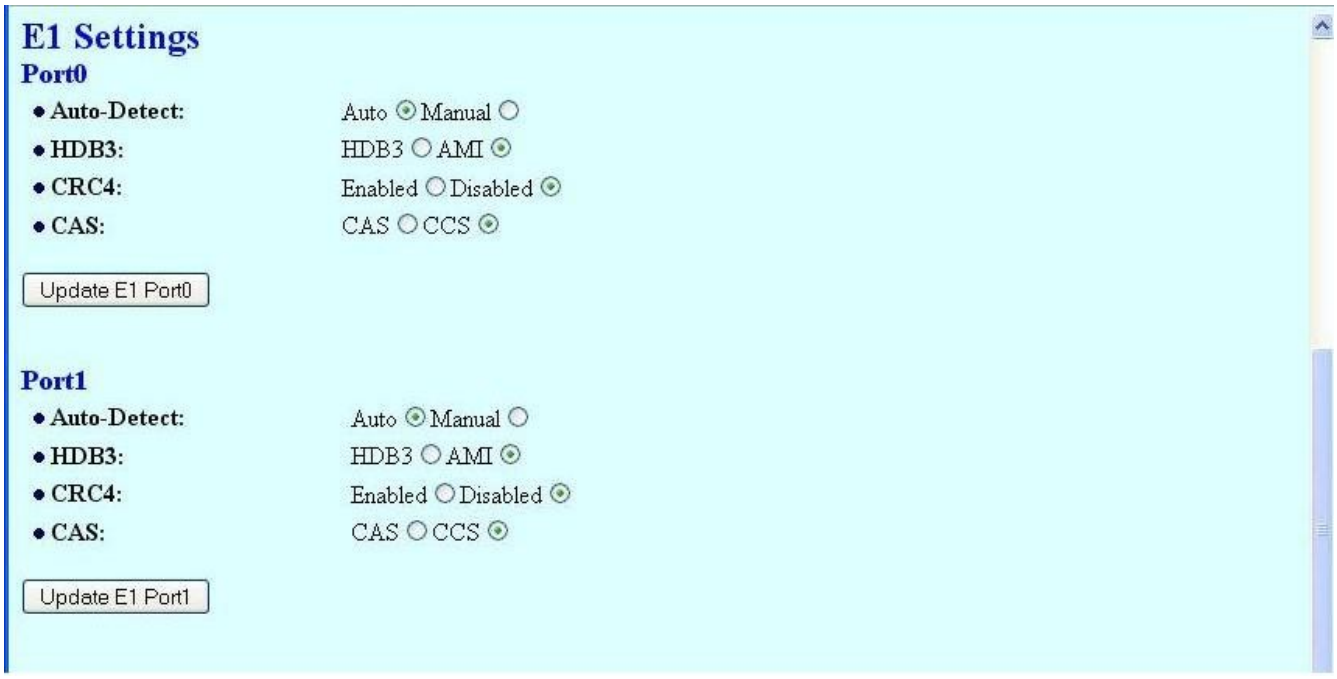


Figure #4 – AVS-1025 E1 Settings

E1 Settings - The E1 setting section provides the user with ability to automatically detect the type of E1 link or to search for a specific type of link. When the E1 setting is set to auto the AVS-1025 will automatically determine the E1 type, signaling type and CRC type. The user can set the AVS-1025 to search for a specific type of E1 by selecting the Manual option along with the specific E1 characteristics then clicking on Update E1 port0/port1.

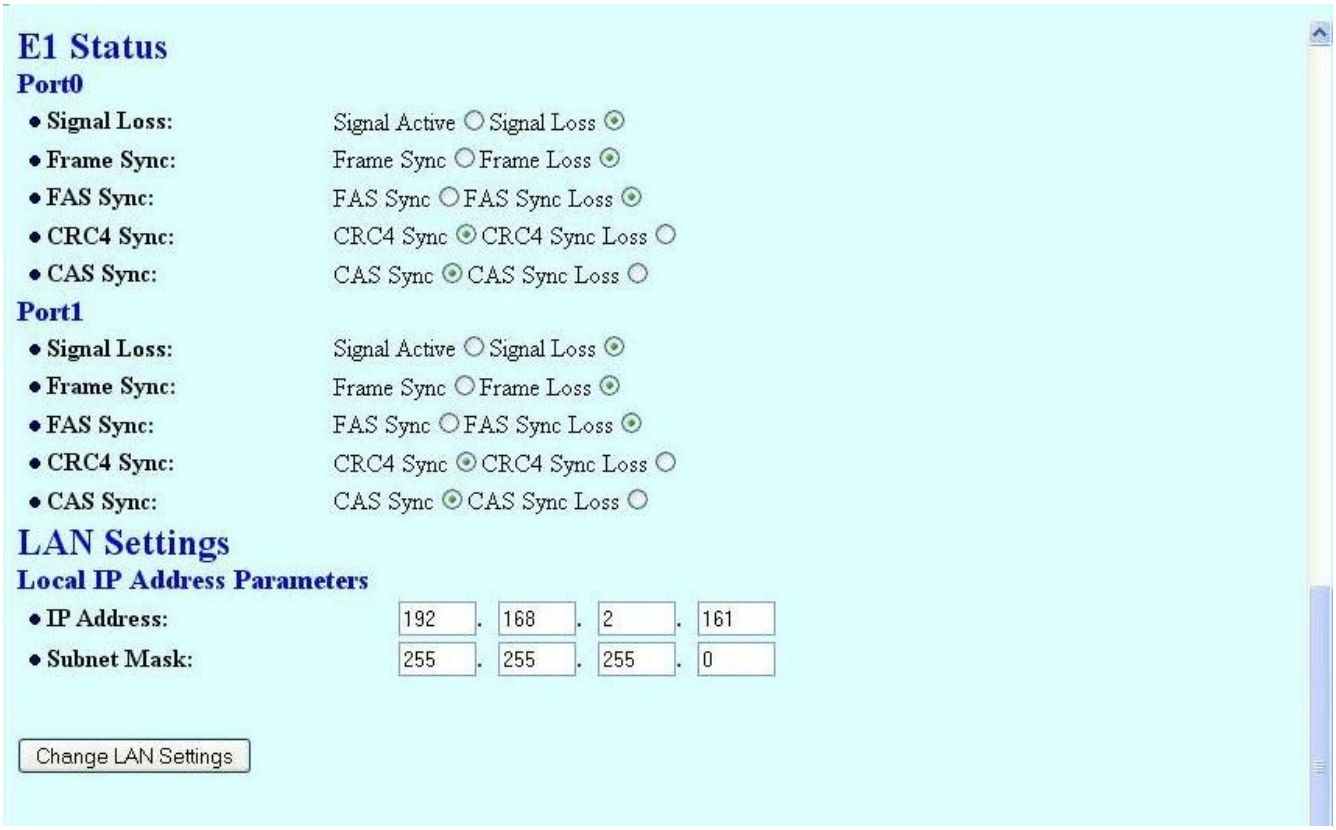


Figure #5 – AVS-1025 E1 Status and LAN Settings

E1 Status -The status of the E1 links are updated each time the user clicks on system settings. The current status of the E1 link is reported as shown above.

Lan Settings – The user can change the IP address and subnet mask. It is necessary to first know the IP address before these settings can be changed.

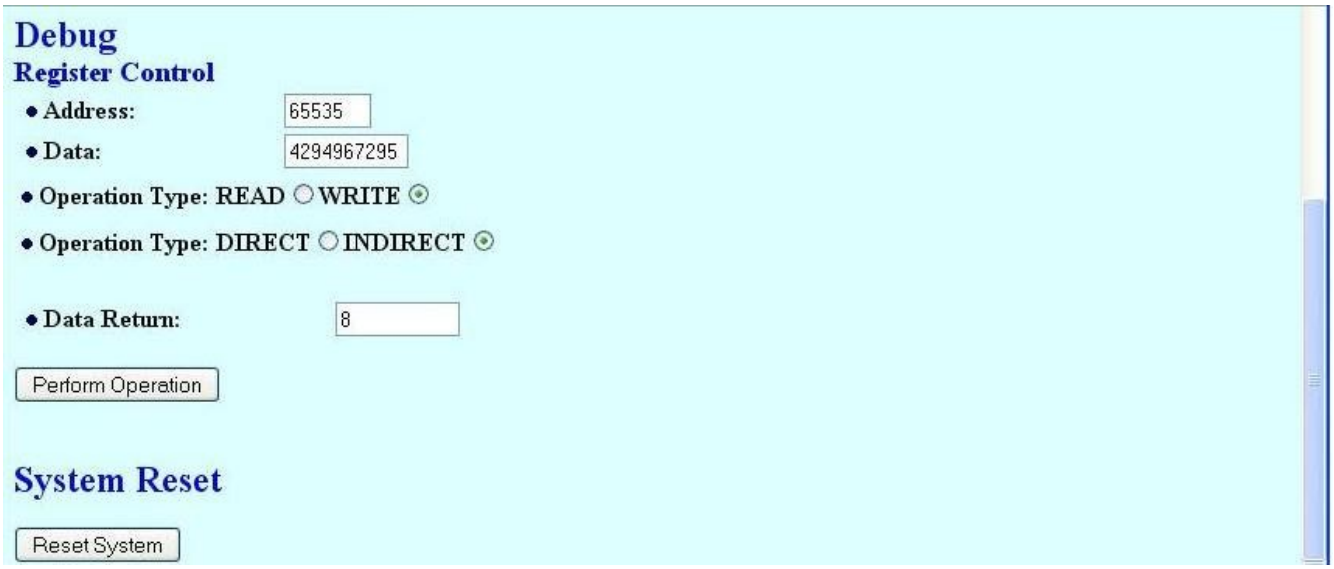


Figure #6 – AVS-1025 Debug and System Reset

Debug – This section is used for the debug of the AVS-1025. This interface is used to to read and write to FPGA addresses in the AVS-1025. This portion of the web page is for debug only and should not be used during normal operation by the operator. Only DIRECT operations should ever be performed and the operator should take great care not to overwrite any board settings when peeking at register values. Appendix 1 contains the register map and descriptions of the pertinent addresses in the FPGA. Address that are not included in the table should not be accessed.

System Reset – System resets restarts the software in the AVS-1025 and reloads the processing FPGA. This reset function does not reset the AVS-1025 back to factory defaults in fact all parameters that have been entered will be written into system flash and will be used after the reset completes.

2.4 Airframe Encoding

The AVS-1025 encodes the E1 up and down link into a flexible airframe that is not dependent on the exact E1 rate. This allows the AVS-1025 transmitter to function on networks that do not have accurate timing. The AVS-1025 transmits E1 data frames when an E1 signal is present and transmits filler data when an E1 link is not present. Filler data can be present on one or both of the E1 data channels. The presences of filler data allows the transmitter and receiver to keep the wireless channel connected even during times when no E1 data links are present. The filler data is a register length 6 linear recursive sequence generated from the shift register structure shown below.

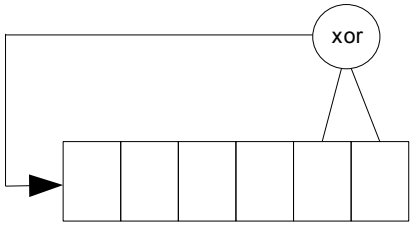


Figure #7 – LRS Generator

The filler data or E1 data is packaged into an air frame as shown in Figure # 8. Six E1 frames of up or down link data are buffered in the AVS-1025. The six frames of E1 or filler data are appended with 160 bits of transmitter status data. This status data identifies the data as filler or E1 data, identifies data as up or down link data and also provides operational data about the transmitter such as transmit power and temperature data. The six frames of data along with the 160 bits of status are then randomized and ½ rate Turbo FEC encoded. After FEC encoding a pre-amble is appended and the data is transmitted. Figure # 8 shows the construction of the air frame.

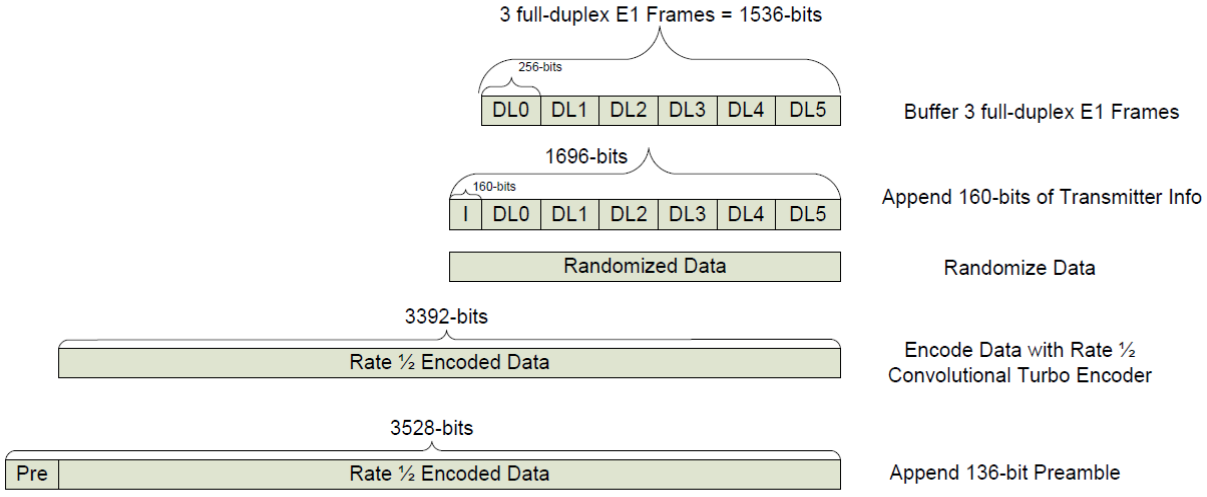


Figure #8 – Airframe Construction

3.0 AVS-1026 E1 Receiver

The receiver is housed in a 3U compact PCI chassis and is comprised of the following:

- AVS-522 Digital Software Defined Radio
- AVS-1026-001 RF Down-converter
- Kontron CP605 Single Board Computer

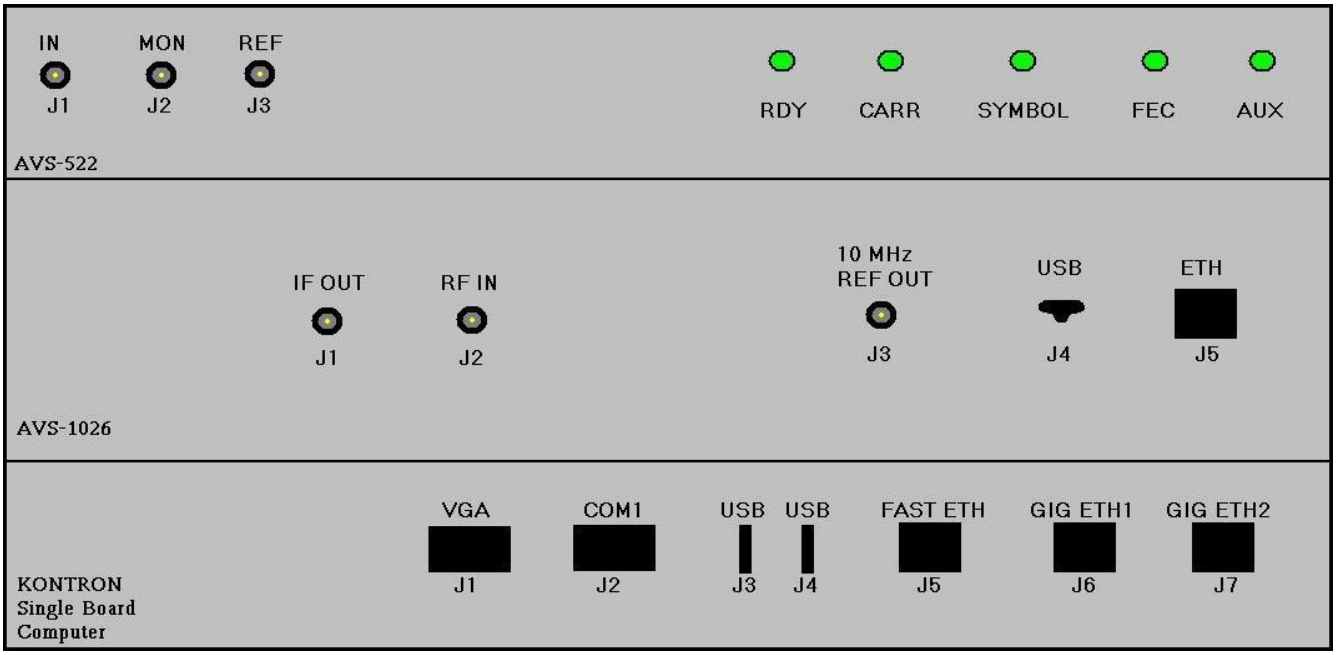


Figure #9 – AVS-1026 Receiver

Jack	Name	Description
J1	IN	70 MHz input, maximum of -20dBm input power
J2	MON	Output monitor of the signal on J1
J3	REF	10 MHz reference clock input

Table #3 – AVS-522 Connector Definitions

LED	Definition
RDY	Bit files loaded to FPGAs
CARR	Carrier lock
SYMBOL	Symbol lock
FEC	FEC lock
AUX	Unused

Table #4 – AVS-522 LED Definitions

Jack	Name	Description
J1	IF Out	70 MHz Intermediate frequency output
J2	RF In	915 MHz Radio frequency input, maximum of -28dBm input power
J3	10 MHz Ref Out	10 MHz Reference clock output
J4	USB	Unused USB interface
J5	ETH	Unused 10 Mbit Ethernet

Table #5 - AVS-1026 Connector Definitions

Jack	Name	Description
J1	VGA	PC Monitor Output
J2	COM1	Unused Serial Port
J3	USB	Keyboard / Mouse
J4	USB	Keyboard / Mouse
J5	FAST ETH	10/100 Ethernet link
J6	GIG ETH 1	Gigabit Ethernet link
J7	GIG ETH 2	Gigabit Ethernet link

Table #6 - Kontron Connector Definitions

The receiver is controlled through the STSC software and GUI. These programs are both launched from their desktop icons. STSC is the interface to the hardware and manages the bit files to be downloaded to the AVS-522. From the GUI, the user can configure the demodulation mode and settings as well as view a constellation plot of the received signal. The user can use J5, J6, or J7 as the E1 data link output via UDP or to control the board remotely.

Once the E1 monitor is powered on and the Windows operating system boots up, the desktop will contain two icons that point to the AVS-1026 GUI and the STSC control software. The STSC control software manages and communicates with the hardware resident in the chassis. The AVS-GUI interfaces with the operator and provides a method to input receiver parameters. The order in which they are launched does not matter but both must be launched for the system to operate.

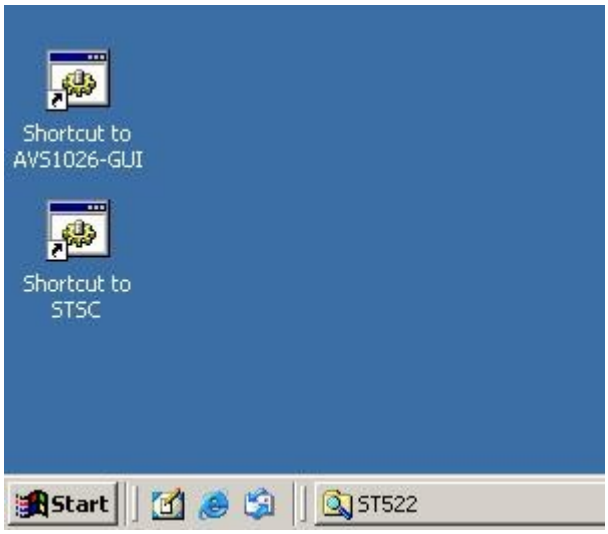


Figure #10 – Receiver Desktop Icons

When the STSC is launched a command window will appear and will start to listen for a GUI process to start. The STSC window will also provide some hardware status such as FPGA programming status etc.

After the GUI is launched, the window in figure #11 will be brought up. This window is the

system control window and gives a quick operational summary of all the receivers in the chassis. The E1 wireless monitor currently uses only one receiver.

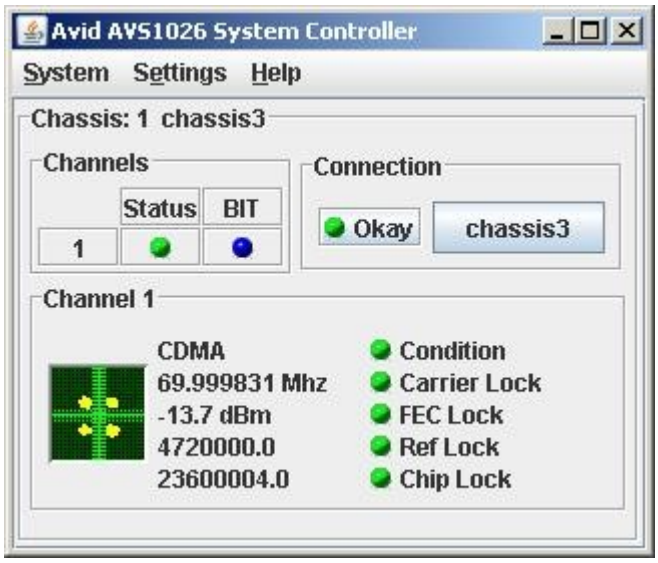
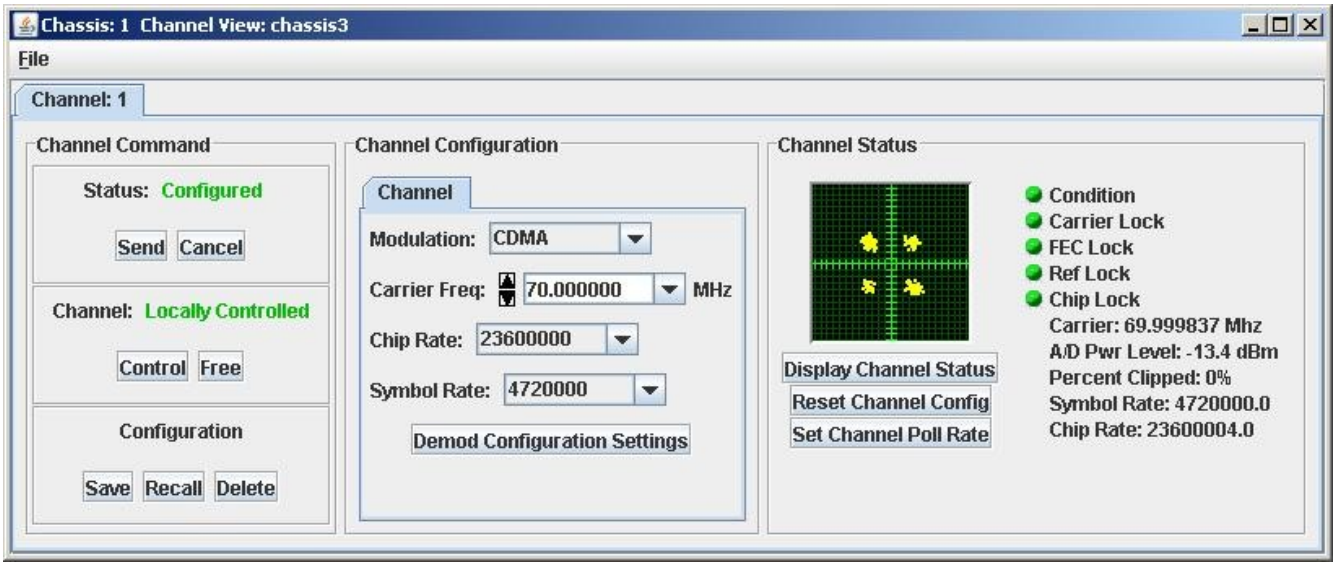


Figure #11 –AVS-1026 GUI System Controller Window

The operator can click anywhere inside this window to launch the channel view window. The channel view is shown in Figure #12 and provides data on a specific receiver in a chassis. The user must first take control of the channel by clicking on the control button. The GUI will then take control of the receiver and the operator will then have the ability to configure the receiver. The user can select modulation type either QPSK or CDMA. When the user selects a different modulation scheme, the GUI alerts the control software of a change in modulation and control software loads the QPSK FPGA bit files. The chip rate and symbol rate pull down menus only have one selection for this application as the E1 monitor only operates at a 4.72 Msps (Mega Symbols Per Second) or 47.2 Mcps (Mega Chips per second). The user can change the intermediate frequency (IF) to which the receiver is tuned by adjusting the Carrier Freq in the GUI. Appendix 2 maps the desired radio frequency (RF) to the nominal Carrier Frequency.

The configuration section of the GUI provides the user with the ability to save, recall and delete specific receiver configurations.



The lights on the right hand side of the GUI provide the user with the current condition of the receiver. Lock conditions such as carrier, symbol and FEC lock are provided. The Ref lock shows that the receiver has locked to a 10MHz reference tone. The constellation plot provides the user with a visual quality of lock condition.

Figure #12 –AVS-1026 GUI Channel View

Selecting the Demod Configuration Setting button in figure #12 will bring up the window shown in figure #13. The Demod Configuration window is a tabbed window that allow the operator to change receiver parameters. The first tab is the board tab. This tab allows the operator to change receiver wide parameters such as Analog Gain, AGC, and AFC modes. The Analog Gain function allows the operator to add an additional 20 dB of gain in the analog front end of the receiver. This should be set to disable unless the operator is sure that the receiver has a very low level signal input to the front end. The Narrow band and Wide band automatic gain control (AGC) can be set to AGC or manual mode. Manual gain mode is most often used when demodulating a burst signal. The E1 wireless monitor should normally use the AGC mode.

The FEC tab normally allows the operator to select variable rate FEC modes, however the E1 wireless monitor only operates in ½ rate Turbo FEC mode and it must be enabled to get functional data from the receiver.

The CDMA tab contains three parameters. The first is synchronous video integrator (SVI) threshold. This provides the number of averages that the receiver will use in the correlators to detect the presence of a spread spectrum waveform. The carrier tracking BW selects the carrier tracking control loop bandwidth. Selection of a narrow loop band width provides better noise performance but a more narrow acquisition band. The loop bandwidth selections are dependent on the operation environment.

The delay lock loop (DLL) filter track band width selects the chip tracking control loop bandwidth. The DLL band can be selected to be narrow in high noise environments and wider in low noise environments. Both the carrier and chip tracking control loops must be enabled for the receiver to track the E1 transmitted signal.

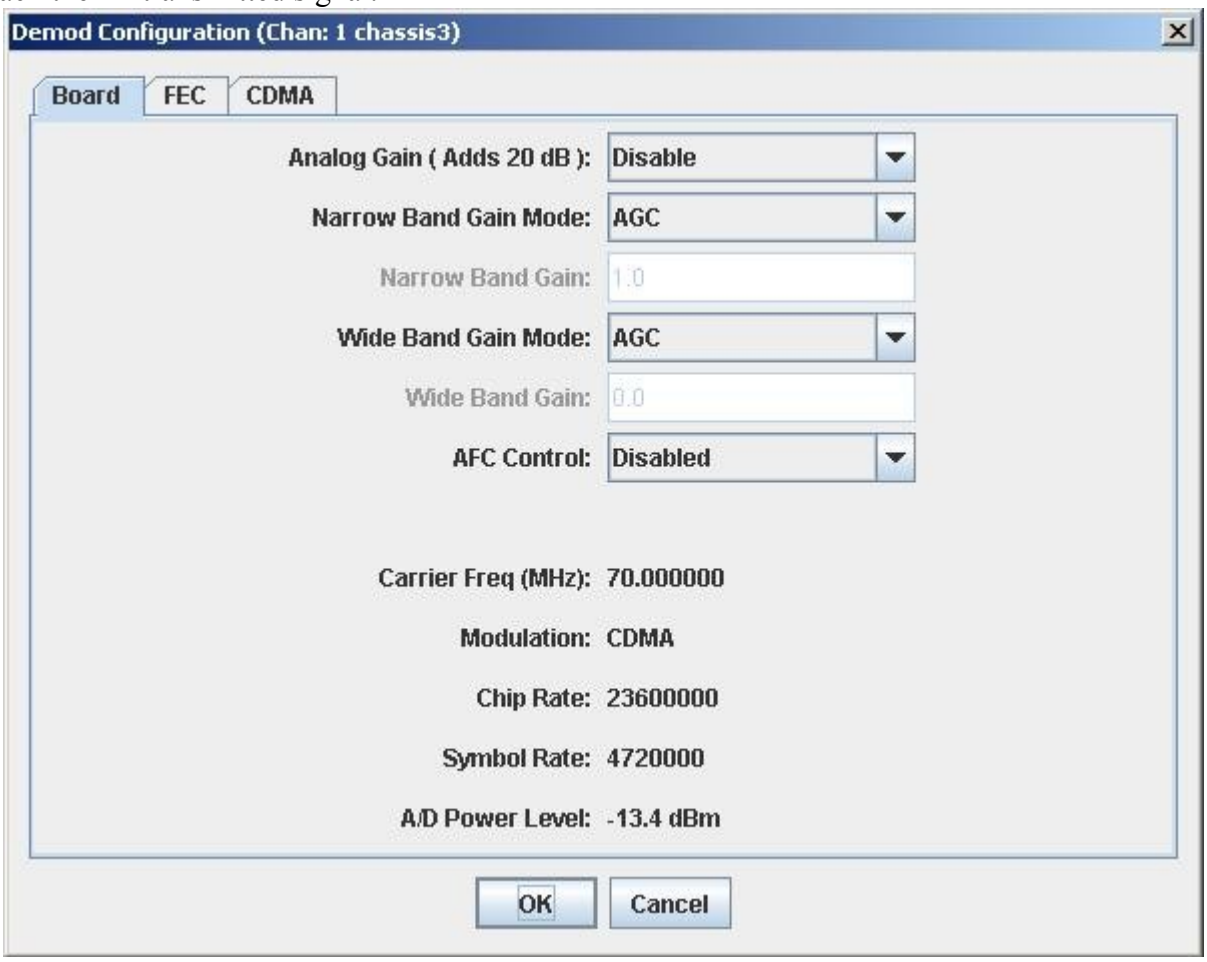


Figure #13 – Demodulation Configuration Settings

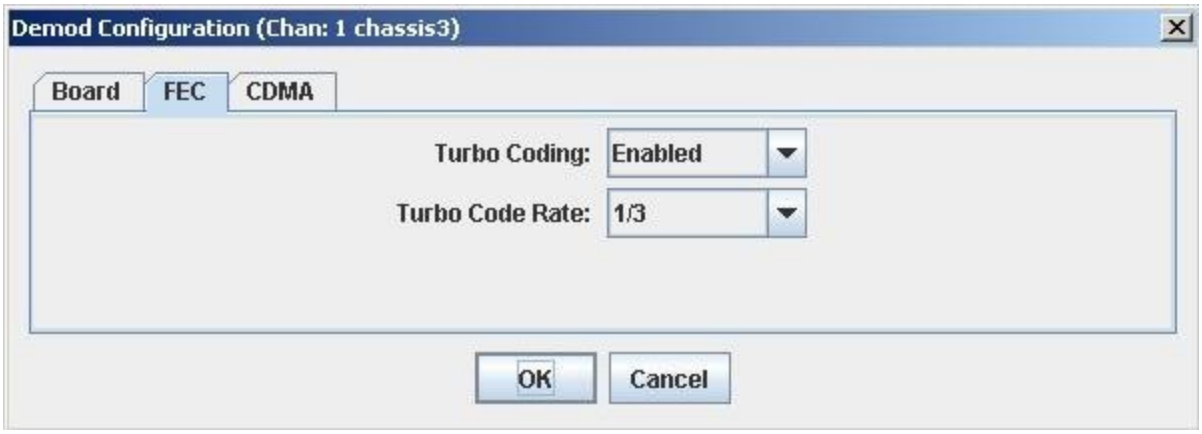


Figure #14– Demodulation Configuration Settings

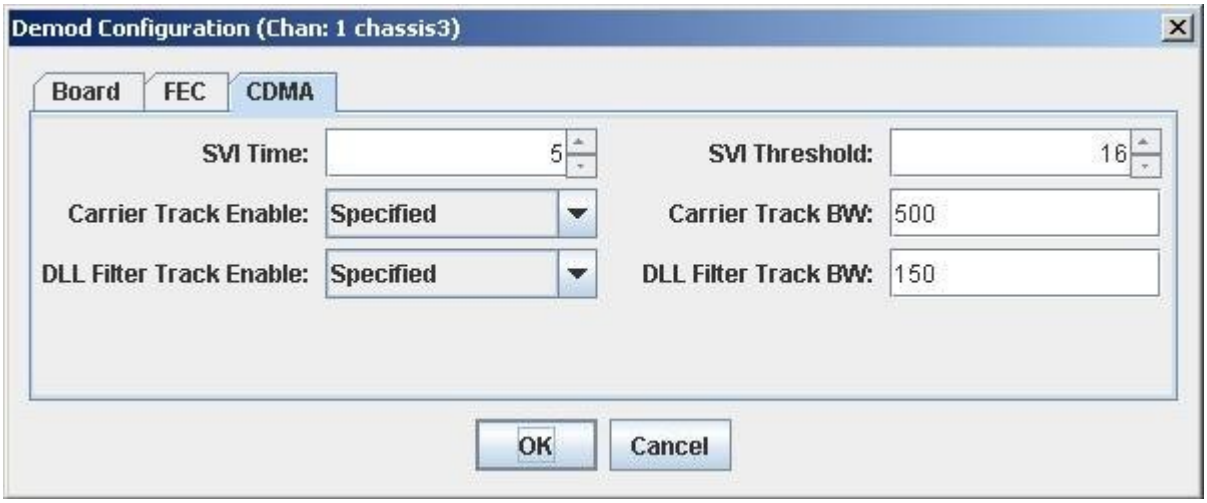


Figure #15 – CDMA Demodulation Configuration Settings

When QPSK modulation is selected the demod configuration menu changes as shown in figure 16. The parameters shown in the QPSK tab are IF track enable, IF Track BW, Symbol Track Enable, and Symbol Track BW. Carrier tracking of the input signal is enabled by selecting specified for the IF track enable. The IF track bandwidth selects the carrier tracking control loop bandwidth. The input signal data transitions are tracked by the symbol tracking control loop. The Symbol Track Enable field must be set to specified for the receiver to track the input signal. The wider bandwidth used in each of these fields provides wider signal acquisition capability but reduced noise rejection.

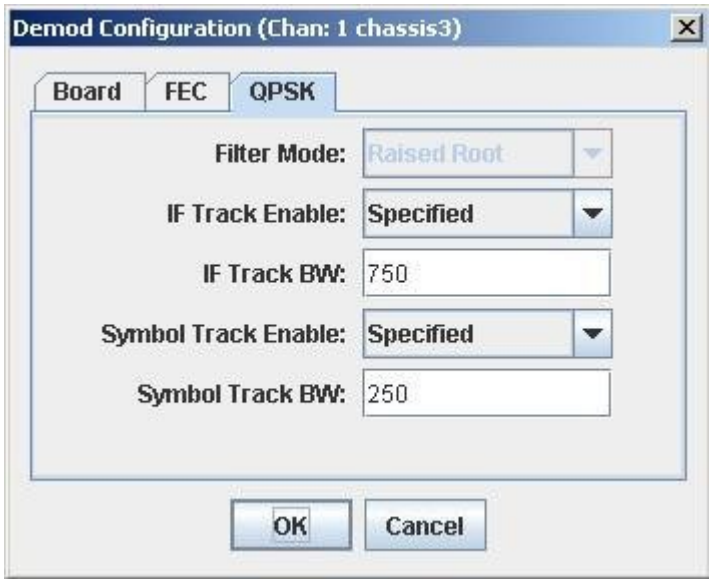


Figure #16 – QPSK Demodulation Configuration Settings

Clicking the "Display Channel Status" button in the Channel window, figure 12, will bring up the status window shown below.

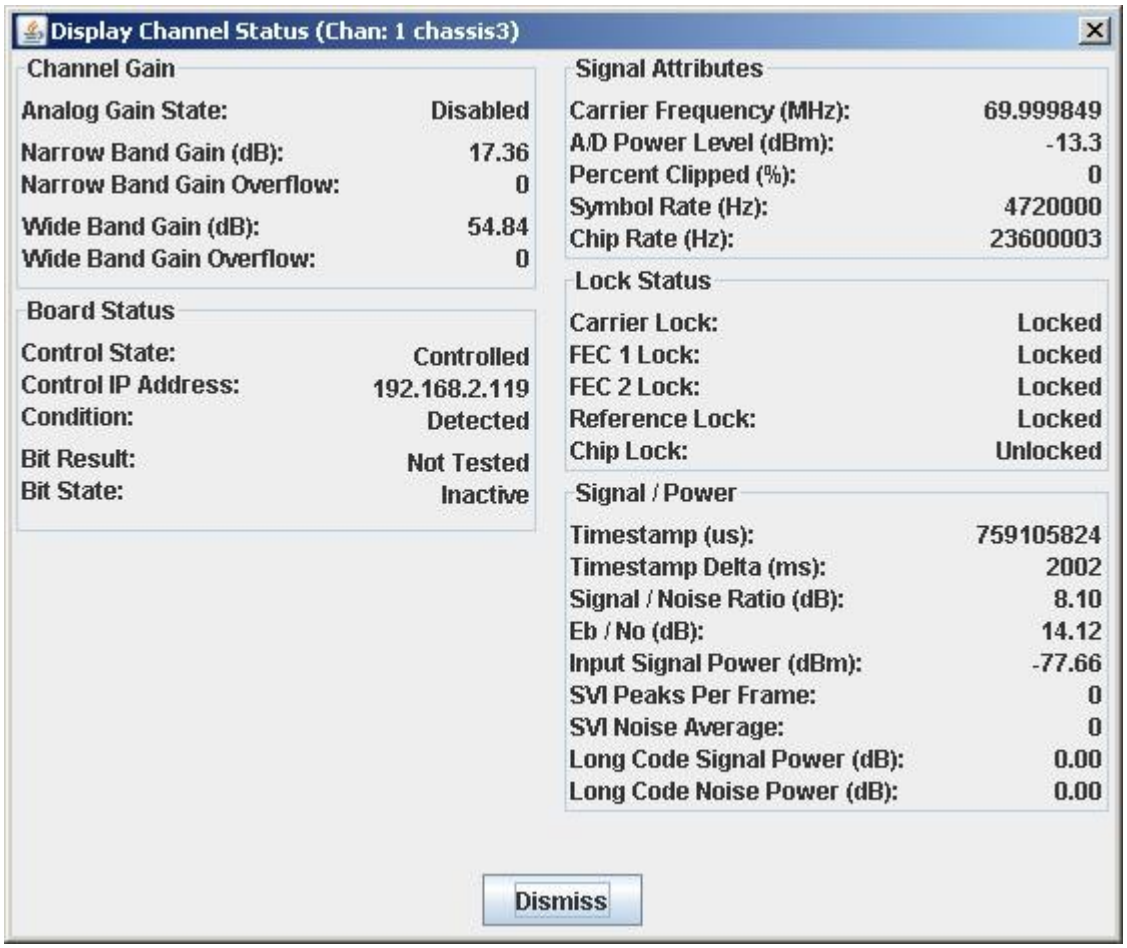


Figure #17 – Channel Status

This window provides various status of the receiver such as power levels to the A to D converter, IP addresses, lock condition, and Eb/No measurements.

4.0 UDPrecv

UDPrecv is a software application written by Avid Systems to demonstrate the Wireless E1 Monitor's capability to forward demodulated and decoded data over an IP network using the UDP protocol. The UDPrecv application receives data from the E1 wireless monitor over an IP network. The UDPrecv application performs two functions. One function of UDPrecv is to receive data from the receiver and write that data to disk. UDPrecv can also be used to display the monitor data that has previously been saved to disk. UDPrecv runs in the Mono framework. Mono is an open source option to the .NET framework. UDPrecv will only run on a computer that has the Mono framework installed. Avid Systems has found that it will also run under the .NET frame work but has not verified that it will run using all versions of .NET. UDPrecv is provided with the Wireless E1 monitor.

4.1 UDPrecv Installation

UDPrecv is installed on any computer that is required to receive data from the Wireless E1 Monitor. UDPrecv needs to run under the MONO framework. To install MONO, run the windows installer executable and follow the installation wizard. Mono is also available for other operating systems at www.mono-project.com.

To install UDPrecv, simply create a UDPrecv folder and copy the udprecv.exe executable into the folder. See section 4.3 for operation of UDPrecv.

4.2 Receiver Configuration

The receiver must be correctly set up to send the UDP data packets. The IP address of the computer and the UDP port need to be specified in the STSC channel configuration file on the AVS-1026 receiver.

To configure STSC to transfer UDP packets, navigate to the directory below on the AVS-1026 receiver. The STSC channel configuration files are located in the following directory:

C:\STSC\config\ST522

Each channel of the receiver has an associated "channel-n.cfg" file which specifies the IP address of the PC running UDPrecv and port which the data will be transferred from. There are two instances of the IP address and port in each channel-n.cfg file. One instance is for QPSK data and the other instance is for transferring DSSS data. Generally, both IP addresses are set to the same value.

The following occurs twice under the Local CDMA and Local QPSK config schemes:

<UdpDestAddress>192.168.2.140</UdpDestAddress>
<UdpDestPort>5150</UdpDestPort>

Edit these lines with the IP address of the PC running UDPrecv and the port at which the UDP

protocol is configured to operate. The default port for the UDP protocol is 5150.

4.3 DMA Transfer Procedure

To use UDPrecv, first setup the receiver with the correct IP address and UDP port for the monitoring computer. Once the IP address and port is set up, launch STSC and the AVS-1026 GUI. Once the receiver is locked, launch UDPrecv.exe on the monitoring computer using the command line below.

--> c:\UDPrecv> mono udprecv.exe

UDPrecv is now running and actively listening for any UDP transfers. (Note: UDPrecv must be running prior to a DMA transfer being initiated on the receiver.)

After UDPrecv is running, a DMA transfer can be initiated on the receiver. The receiver is configured to use DMA only when it is commanded to do so. To start a DMA transfer of E1 airframe data from the receiver to the monitoring computer, type the following in the STSC command window on the AVS-1026 receiver:

--> >>> dmastart 0

and

--> >>> dmastop 0

to stop the transfer. The integer 0 in both commands denotes the receiver channel.

Once the DMAstart command has been issued, the UDPrecv window will print the "filename" it has created indicating it is processing an active transfer. In the UDPrecv window, once the DMA transfer has been stopped, use Crtl-c to halt the UDPrecv program. UDPrecv generates a binary file that can be post processed.

UDPrev also provides the ability to process the binary file that was created and display it to the screen in human readable format with the following command.

--> c:\udprecv> mono udprecv.exe "filename"

To pipe the "filename" to a formatted file of your choosing, in the UDPrecv window use:

--> c:\udprecv> mono udprecv.exe "filename" > untitled.dat

Using a text editor to view the output data you can see the following structure. Each UDP packet consists of an 11-byte header which is parsed and displayed at the top of the data followed by either 5 or 6 airframe packets. The airframe packet is grouped into 32-bit words. Each airframe consists of a 5 word (20 byte) status header and 48 words of either Port 0 (UL) or Port 1 (DL) data.

```
File: G000R000.0073
UDP 0001 DMA 0000: Type=01 GRU=00 RECVR=00
  AF000
    FF300108 2105D307 00000000 00000000 00000000 5FAAAAAA AAAAAAAA AAAAAAAA
    AAAAAAAA FFAAAAAA AAAAAAAA AAAAAAAA AAAAAAAA 9BAAAAAA AAAAAAAA AAAAAAAA
    AAAAAAAA FFAAAAAA AAAAAAAA AAAAAAAA AAAAAAAA DFAAAAAA AAAAAAAA AAAAAAAA
    AAAAAAAA FFAAAAAA AAAAAAAA AAAAAAAA AAAAAAAA 1BAAAAAA AAAAAAAA AAAAAAAA
    AAAAAAAA FFAAAAAA AAAAAAAA AAAAAAAA AAAAAAAA DFAAAAAA AAAAAAAA AAAAAAAA
    AAAAAAAA FFAAAAAA AAAAAAAA AAAAAAAA AAAAAAAA 1BAAAAAA AAAAAAAA AAAAAAAA
    AAAAAAAA FFAAAAAA AAAAAAAA AAAAAAAA AAAAAAAA

  AF001
    F0300108 2105D307 00000000 00000000 00000000 9BAAAAAA AAAAAAAA AAAAAAAA
    AAAAAAAA FFAAAAAA AAAAAAAA AAAAAAAA AAAAAAAA DFAAAAAA AAAAAAAA AAAAAAAA
    AAAAAAAA FFAAAAAA AAAAAAAA AAAAAAAA AAAAAAAA 1BAAAAAA AAAAAAAA AAAAAAAA
    AAAAAAAA FFAAAAAA AAAAAAAA AAAAAAAA AAAAAAAA DFAAAAAA AAAAAAAA AAAAAAAA
    AAAAAAAA FFAAAAAA AAAAAAAA AAAAAAAA AAAAAAAA 1BAAAAAA AAAAAAAA AAAAAAAA
    AAAAAAAA FFAAAAAA AAAAAAAA AAAAAAAA AAAAAAAA DFAAAAAA AAAAAAAA AAAAAAAA
    AAAAAAAA FFAAAAAA AAAAAAAA AAAAAAAA AAAAAAAA
```

Figure #18 – Parsed UDP Receive Packet Data

The following table describes the airframe header. It is 5 32-bit words or 20 bytes in length.

Byte	Name	Bit Definitions
0	Data Type / Port ID	Bit 7:4 “0000” = Filler Data “1111” = Live E1 Data Bit 3:0 “0000” = Port 0 “1111” = Port 1
1	E1 Link Status	Bit 7 “1” = Frame Loss Bit 6 “1” = Signal Loss Bit 5 “1” = Received Signal Loss Bit 4 “1” = E1 Link Good Bit 3:0 “0000”
2	E1 Link Good	Bit 7:1 “0000000” Bit 0 “1” = E1 Link Good
3	Power Meas. MSB	Bit 7:0 Transmit power measurement MSB
4	Power Meas. LSB	Bit 7:0 Transmit power measurement LSB
5	Temp Meas MSB	Bit 7:0 Transmitter temperature measurement MSB
6	Temp Meas LSB	Bit 7:0 Transmitter temperature measurement LSB
7	E1 Link Type	Bit 7:3 “0000” Bit 2 “1” = CAS “0” = CCS Bit 1 “1” = CRC4 Enable “0” = CRC4 Disabled Bit 0 “1”= HDB3 “0” = AMI
8 --18	Not Used	All zeros
19	Link Packet Counter	Bit 7:0 Packet Count for the specified UL/DL channel.

Table 8: Airframe Status Header Definitions

5.0 UDP Packet Header Description

The E1 Data is sent from the receiver to the user via UDP packets. The UDP packets are described in this section. Figure #19 shows the UDP packet structure.

Figure #19 -UDP Packet

The UDP packet is made up of an 11 byte header and a variable size payload. The size of the payload can be calculated from data contained in the 11 byte header.

The UDP packet header is defined below in Figure #20.

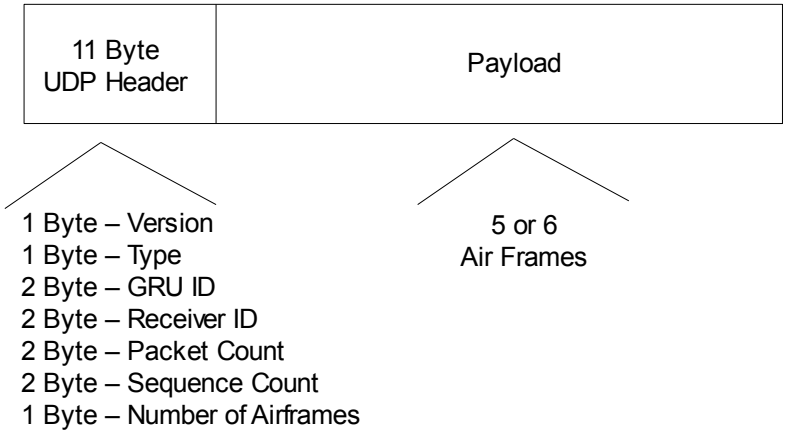


Figure #20 – UDP Packet Header

The UDP header is made up of an eleven byte field as defined below:

Version – This single byte field denotes the version of the UDP packet definition. This field was created to provide backward compatibility of any changes to the UDP packet structure.

Type – Single Byte Field that is currently set to a 1 and denotes that the transmitted data is Air Frame data.

GRU ID – GRU (Ground Receiver Unit) a two byte field that identifies the chassis which the UDP data is sourced from.

Receiver ID – This two byte field identifies the receiver number that is sourcing the UDP data. Currently, this system is only a single receiver system.

Packet Count – This two byte count is sourced from the receiver and counts the number of DMA buffers that the receiver has filled. This count was mainly used for debugging to ensure all data was being transferred. This count approximately increments 1 for every 13 UDP packets transferred.

Sequence Count – This two byte count counts the number of UDP packets sent from the receiver. This count is useful in identifying dropped packets which can occur on a busy network.

Number of Air Frames – This single byte value identifies the number of Air Frames that are contained in the UDP payload.

5.1 Air Frame Description

The Air Frame contained in each UPD packet is a 53 word data structure and is shown in Figure #21. The Air Frame starts with a 5 word (1 word = 4 bytes) status word. The status word provides information about the data contained in the Air Frame such as is it up or down link E1 data and if the data is filler data or actual E1 data. The status word also contains information about the transmitter such as transmit power, and temperature.

Air Frame = 53 Words

The 5 Word status field is defined in Table #8. The status word is highlighted in Table #9 in blue. The first word in the status field is 0xFF300108 this word is broken down below to better define the bit definitions.

Break Down

F – First nibble signifies that this data is live E1 data. If this nibble were a 0 it would signify that the data contained in the Air Frame is filler data.

F - Second nibble identifies which channel this data was sourced from. F signifies that this data is from port 1. A zero would indicate that the data was from port 0.

0x30 - Indicates E 1 link status.

0x01 – Indicates that the E1 link is good.

0x08 – Most significant byte of the measured transmit power.

The second word of the status word is 0x 2105D307

0x21 – LSB of the measured transmit power.

0x05 – MSB of the transmitter temperature.

0xD3 – LSB of the transmitter temperature

0x07 – E1 link data

Words 8 through 18 are unused. Word 19 is an Air Frame counter. This counts the number of airframes sent from the up and down link channels.

A single E1 frame is shown below.

```
5FAAAAAA AAAAAAAA AAAAAAAA  AAAAAAAA FFAAAAAA AAAAAAAA AAAAAAAA AAAAAAAA
```

```
File: G000R000.0073
UDP 0001 DMA 0000: Type=01 GRU=00 RECVR=00
  AF000
    FF300108 2105D307 00000000 00000000 00000000 5FAAAAAA AAAAAAAA AAAAAAAA
    AAAAAAAA FFAAAAAA AAAAAAAA AAAAAAAA AAAAAAAA 9BAAAAAA AAAAAAAA AAAAAAAA
    AAAAAAAA FFAAAAAA AAAAAAAA AAAAAAAA AAAAAAAA DFAAAAAA AAAAAAAA AAAAAAAA
    AAAAAAAA FFAAAAAA AAAAAAAA AAAAAAAA AAAAAAAA 1BAAAAAA AAAAAAAA AAAAAAAA
    AAAAAAAA FFAAAAAA AAAAAAAA AAAAAAAA AAAAAAAA DFAAAAAA AAAAAAAA AAAAAAAA
    AAAAAAAA FFAAAAAA AAAAAAAA AAAAAAAA AAAAAAAA 1BAAAAAA AAAAAAAA AAAAAAAA
    AAAAAAAA FFAAAAAA AAAAAAAA AAAAAAAA AAAAAAAA

  AF001
    F0300108 2105D307 00000000 00000000 00000000 9BAAAAAA AAAAAAAA AAAAAAAA
    AAAAAAAA FFAAAAAA AAAAAAAA AAAAAAAA AAAAAAAA DFAAAAAA AAAAAAAA AAAAAAAA
    AAAAAAAA FFAAAAAA AAAAAAAA AAAAAAAA AAAAAAAA 1BAAAAAA AAAAAAAA AAAAAAAA
    AAAAAAAA FFAAAAAA AAAAAAAA AAAAAAAA AAAAAAAA DFAAAAAA AAAAAAAA AAAAAAAA
    AAAAAAAA FFAAAAAA AAAAAAAA AAAAAAAA AAAAAAAA 1BAAAAAA AAAAAAAA AAAAAAAA
    AAAAAAAA FFAAAAAA AAAAAAAA AAAAAAAA AAAAAAAA DFAAAAAA AAAAAAAA AAAAAAAA
    AAAAAAAA FFAAAAAA AAAAAAAA AAAAAAAA AAAAAAAA
```

Table #9 – Air Frame Structure

AF000 – Air Frame Count

6 E1 Frames are shown in green.

Appendix 1

Appendix 1 Details the DIRECT register space of the AVS-1025 transmitter FPGA. These registers can be helpful when troubleshooting the operation of the transmitter. These registers should only be read, to ensure normal operation of the transmitter. If write are required to debug an issue, the transmitter should be powered down and back up to ensure normal operation has resumed. Table 9 contains the register names, addresses, and descriptions. The user must ensure the the DIRECT radio button is activated in the user interface before any debug access are performed.

Register	Address (Decimal)	Access Read Only = R Write/Read = WR	Description
Test Register	0	WR	This is an 16-bit test register that can be used to test communication between the mico-controller and the FPGA. Note, writes to this register do not affect the operation of the transmitter.
FPGA DCM Lock Status Register	7	R	Contains the lock status of the Digital Clock Managers within the FPGA. A value of 1 in each bit indicates that the DCM is locked. BIT2 – DAC Data Clock DCM Lock Indication BIT1 – 188.8MHz DCM Lock Indication BIT0 – E1 16.384MHz DCM Lock Indication
Digital PLL Lock Status Register	8	R	A value of 1 in this register indicates that the digital PLL is locked, a 0 indicates that the PLL is unlocked.
RF PLL Lock Status Register	16	R	A value of 1 in this register indicates that the RF PLL is locked, a 0 indicates that the PLL is unlocked.
FPGA Version Register	17	R	FPGA version register is 16-bits. The upper byte contains the major version of the FPGA load and the lower byte contains the minor version of the FPGA load.
E1 UL Good Register	18	WR	This register allows the microcontroller to let the FPGA know when the E1 transceiver has synchronized to an E1 signal on the UL (Port0) by setting the register to a value of 1.
E1 DL Good Register	19	WR	This register allows the microcontroller to let the FPGA know when the E1 transceiver has synchronized to an E1 signal on the DL (Port1) by setting the register to a value of 1.
E1 UL FRM Loss Register	20	R	This register is set by the FPGA when it has synchronized to the UL (port0) data from the E1 transceiver.
E1 DL FRM Loss Register	21	R	This register is set by the FPGA when it has synchronized to the DL (port1) data from the E1 transceiver.
E1 UL Type Register	22	R	Indicates the UL E1 type detected in auto-detect mode. 7 = HDB3, CRC-4, CAS 6 = HDB3, CRC-4, CCS 5 = HDB3, NO CRC-4, CAS 4 = HDB3 ONLY 0 = AMI 8 = No E1 Signal Detected
E1 DL Type Register	23	R	Indicates the DL E1 type detected in auto-detect mode. 7 = HDB3, CRC-4, CAS 6 = HDB3, CRC-4, CCS 5 = HDB3, NO CRC-4, CAS 4 = HDB3 ONLY 0 = AMI 8 = No E1 Signal Detected
Modulation Mode Register		WR	1 indicates that the FPGA has been configured for spread spectrum modulation and 0 indicates that the FPGA has been configured for QPSK modulation.

Table 10: FPGA Register Map

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Appendix 2

Currently the transmitter RF frequency is defined at RF centered at 915MHz and the receiver frequency is tuned to the transmitter by adjusting the IF frequency. Table 10 associates the transmitter RF frequency the nominal receiver IF frequency setting required to lock the receiver to the transmitter. Note that the transmitter should be set for 915MHz and the receiver should be set for 70MHz at all times when they are configured for spread spectrum mode. The equation used to calculation the appropriate receiver frequency base on the desired RF frequency is below.

Carrier Freq = 70MHz + (915MHz – DesiredRF)

e.g.,

If we desire an RF frequency of 910MHz, then

Carrier Freq = 70MHz + (915MHz – 910MHz)
Carrier Freq = 70MHz + (5MHz)
Carrier Freq = 75MHz

Transmitter Radio Frequency (RF) in MHz	Receiver Carrier Frequency, IntermediateFrequency (IF) in MHz
933	52
932	53
931	54
930	55
929	56
928	57
927	58
926	59
925	60
924	61
923	62
922	63
921	64
920	65
919	66
918	67
917	68
916	69
915	70
914	71
913	72
912	73
911	74
910	75
909	76
908	77
907	78
906	79
905	80
904	81
903	82
902	83
901	84
900	85
899	86
898	87
897	88

Table 10: Transmitter/Receiver Frequency Settings