AVID SYSTEMS
Signal Processing & Communications Systems

AVS-006 Application Note

The AVS-006 uses an inexpensive FPGA and a series of phase look loop circuits to produce a low phase noise arbitrary output frequency. The AVS-006 is used to provide a clock output that is phase locked to the input 10 MHz reference but does not have an integer relation in frequency. The block diagram of the AVS-006 is shown below.

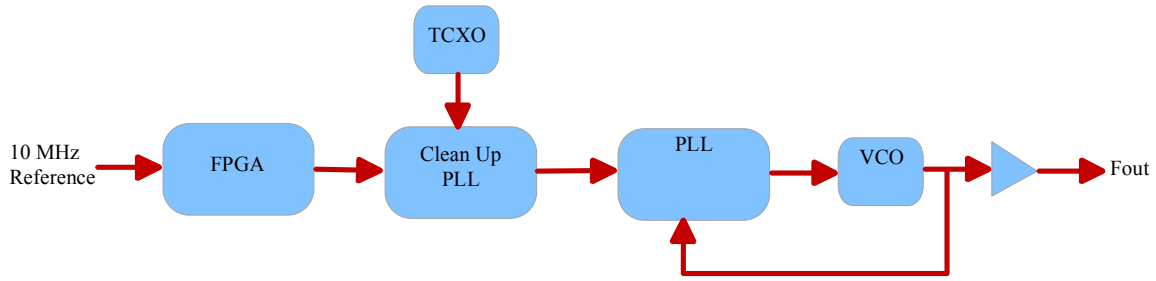

Figure 1 – AVS-006 Block Diagram

Applications such as direct digital synthesizers (DDS) need to be locked to an external reference in order to assure that the output frequency is accurate. However, even when using an external reference, DDSs exhibit frequency error due to the DDS architecture itself. The DDS shown in figure #2 uses a 32 bit numerically controlled oscillator (NCO) to address a sine/cosine look up table (LUT). The NCO shown in figure #2 increments by a fixed value depending on the required output frequency of the DDS. The NCO value represents the phase increment of the sinusoid that will be produced by the DDS. Frequency is related to phase as follows:

$$\omega = d\Phi/dt \qquad \text{eq. 1}$$

In the formula above, the phase increment $d\Phi$ is simply the input phase increment and dt is 1/fs, the rate at which the NCO is running. Making these substitutions yields the following:

$$\omega = \text{phase increment} * fs \qquad \text{eq. 2}$$

Knowing that $\omega = 2\pi f$ the equation above can be used to compute the output frequency of the DDS.

$$2\pi f = \text{phase increment} * fs \qquad \text{eq. 3}$$

Sinusoids repeat every 2π radians. In the case of a DDS 2π is then represented by 2^number of NCO bits since the look up table will be traversed every 2^number of NCO bits. In the case in figure #2 2π is represented by 2^32 since the NCO has 32 bits. This yields the following

fout = (phase increment * fs)/2^32 eq. 4

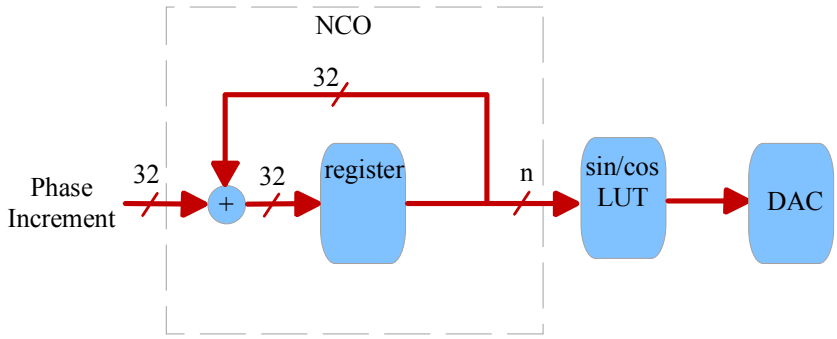

Figure #2 – DDS Architecture

From eq. 4 the source of the error from a DDS is the ratio of fs/2^number of NCO bits. This error is quite low when an NCO with 32 bits or more is used but in some cases such as in the case when a DDS is used in test equipment an exact output frequency is needed. In order to eliminate the frequency error of a DDS the sample rate, fs, must be a power of 2.

The AVS-006 automatically selects the external 10 MHz reference if it is available or selects the internal reference when the external reference is not present. The FPGA uses an internal PLL to multiply the input reference frequency up by a factor of 64 and then divide by 25. This yields a clock frequency of 25.6 MHz. The 25.6 MHz clock is then input to a second FPGA based PLL that is set to multiply by 32 and divide by 25 yielding a clock frequency of 32.768 MHz. The 32.768 MHz clock is then output from the FPGA to a clean up PLL. The cleanup PLL removes the jitter from the clock generated from the FPGA. The cleaned up clock is them used as the reference to an integer PLL circuit that controls a VCO that can now be programmed to have a power of 2 output frequency. The output of the AVS-006 can be used to source a DDS with a clock frequency that is a power of 2 for zero error operation.

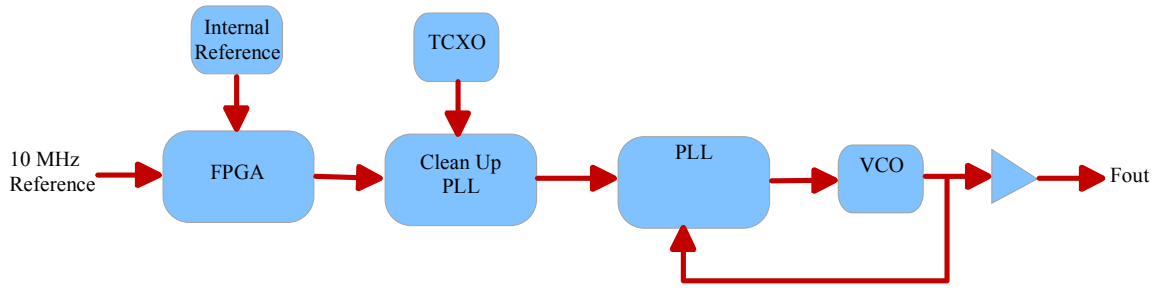

Figure #3 – AVS-006 Block Diagram.


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